VLA500-01 Hybrid Gate Driver Application Information

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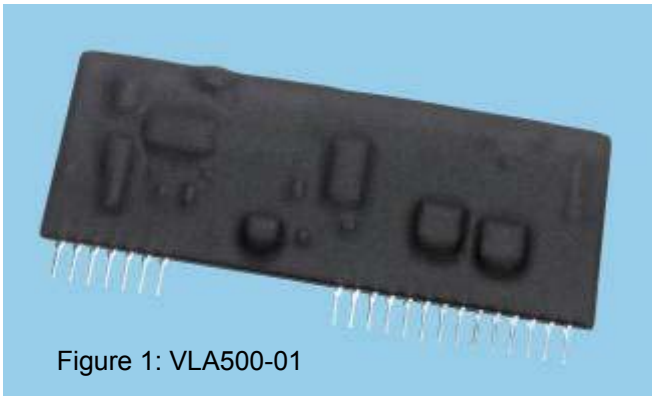
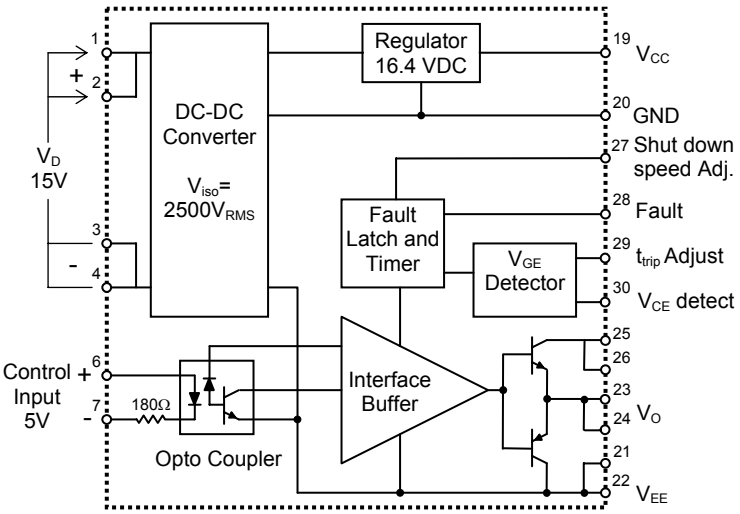


Figure 1: VLA500-01

Figure 2: VLA500-01 Block Diagram



1. General Description

The VLA500-01 is a hybrid integrated circuit designed to provide gate drive for high power IGBT modules. This circuit has been optimized for use with Powerex NF-Series and A-Series IGBT modules. However, the output characteristics are compatible with most MOS gated power devices. The VLA500-01 features a compact single-in-line package design as shown in figure 1. The upright mounting design minimizes required printed circuit board space to allow efficient flexible layout. A block diagram showing the main features of the VLA500-01 is shown in figure 2. The VLA500-01 converts logic level control signals into fully isolated +15V/-8V gate drive with up to 12A of peak drive current. Isolated drive power is provided by a built in DC to DC converter and control signal isolation is provided by an integrated high speed opto-coupler. Short circuit protection is provided by means of destauration detection. This application note will describe the features and operation of the VLA500-01 in detail.

2. Short Circuit Protection

Most Powerex IGBT modules are designed to survive low impedance short circuits for a minimum of 10μs. In order to take full advantage of this capability it is often desirable to include fast acting protection as part of the gate drive circuit. Implementing the protection as part of the gate drive circuit helps to provide faster response by eliminating the propagation delays of the controller. The VLA500-01 provides short-circuit protection by means of an on-state collector to emitter voltage sensing circuit. This type of protection is often called "***desaturation detection***". The operation of this protection circuit is described in this section.

2.1. Desaturation Detection

Figure 3 shows a block diagram of a typical desaturation detector. In this circuit, a high voltage fast recovery diode (D1) is connected to the IGBT's collector to monitor the collector to emitter voltage. When the IGBT is in the off state, V_{CE} is high and D1 is reverse biased. With D1 off the (+) input of the comparator is pulled up to the positive gate drive power supply (V+) which is normally +15V. When the IGBT turns on, the comparator's (+) input is pulled down by D1 to the IGBT's $V_{CE(sat)}$. The (-) input of the comparator is supplied with a fixed voltage (V_{TRIP}). During a normal on-state condition the comparator's (+) input will be less than V_{TRIP} and its output will be low. During a normal off-state condition the comparator's (+) input will be larger than V_{TRIP} and its output will be high. If the IGBT turns on into a short circuit, the high current will cause the IGBT's collector-emitter voltage to rise above V_{TRIP} even though the gate of the IGBT is being driven on. This abnormal presence of high V_{CE} when the IGBT is supposed to be on is often called ***desaturation***. Desaturation can be detected by a logical AND of the driver's input signal and the comparator output. When the output of the AND goes high a short circuit is indicated. The output of the AND can be used to command the IGBT to shut down in order to protect it from the short circuit. A delay (t_{TRIP}) must be provided after the comparator output to allow for the normal turn-on time of the IGBT. The t_{TRIP} delay is set so that the IGBT's Vce has enough time to fall below V_{TRIP} during normal turn-on switching. If t_{TRIP} is set too short, erroneous desaturation detection will occur. The maximum allowable t_{TRIP} delay is limited by the IGBT's short-circuit withstanding capability. In typical applications using Powerex IGBT modules the recommended limit is 10us.

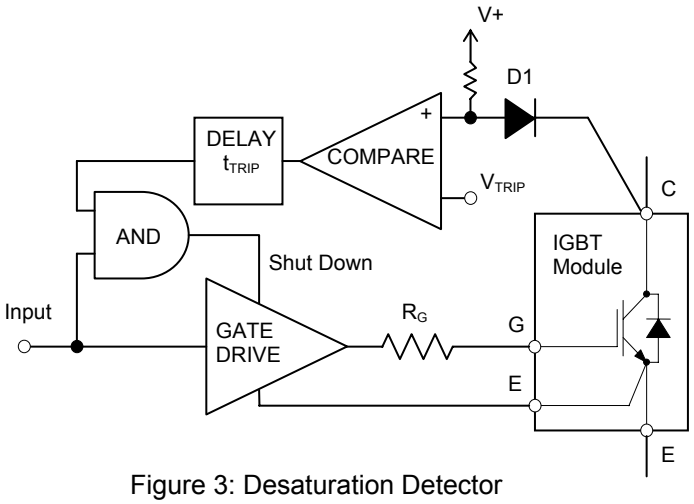


Figure 3: Desaturation Detector

2.2 Operation of the VLA500-01 Desaturation Detector

The Powerex VLA500-01 incorporates short-circuit protection using desaturation detection as described above. A flow chart for the logical operation of the short-circuit protection is shown in Figure 4. When desaturation is detected the hybrid gate driver performs a soft shut down of the IGBT and starts a timed (t_{timer}) 1.5ms lock out. The soft turn off helps to limit the transient voltage that may be generated while interrupting the large short circuit current flowing in the IGBT. During the lock out the driver pulls pin 28 low to indicate the fault status. Normal operation of the driver will resume after the lock-out time has expired and the control input signal returns to its off state.

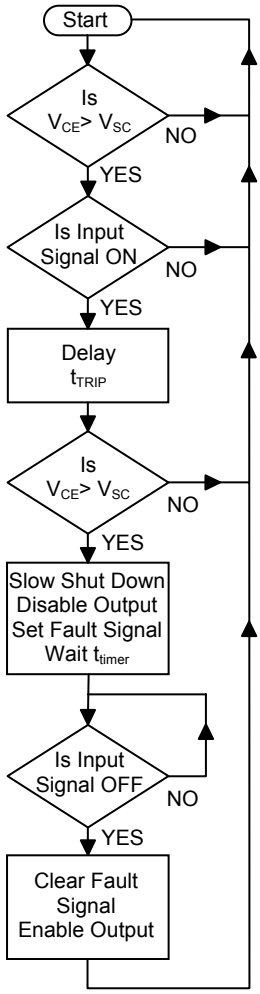


Figure 4: VLA500-01 Desaturation Detector Operation

2.3 Adjustment of Trip time

The VLA500-01 has a default short-circuit detection time delay (t_{TRIP}) of approximately 3µs. This will prevent erroneous detection of short-circuit conditions as long as the series gate resistance (R_G) is near the minimum recommended value for the module being used. The 3µs delay is appropriate for most applications so adjustment will not be necessary. However, in some low frequency applications it may be desirable to use a larger series gate resistor to slow the switching of the IGBT, reduce noise, and limit turn-off transient voltages. When R_G is increased, the switching

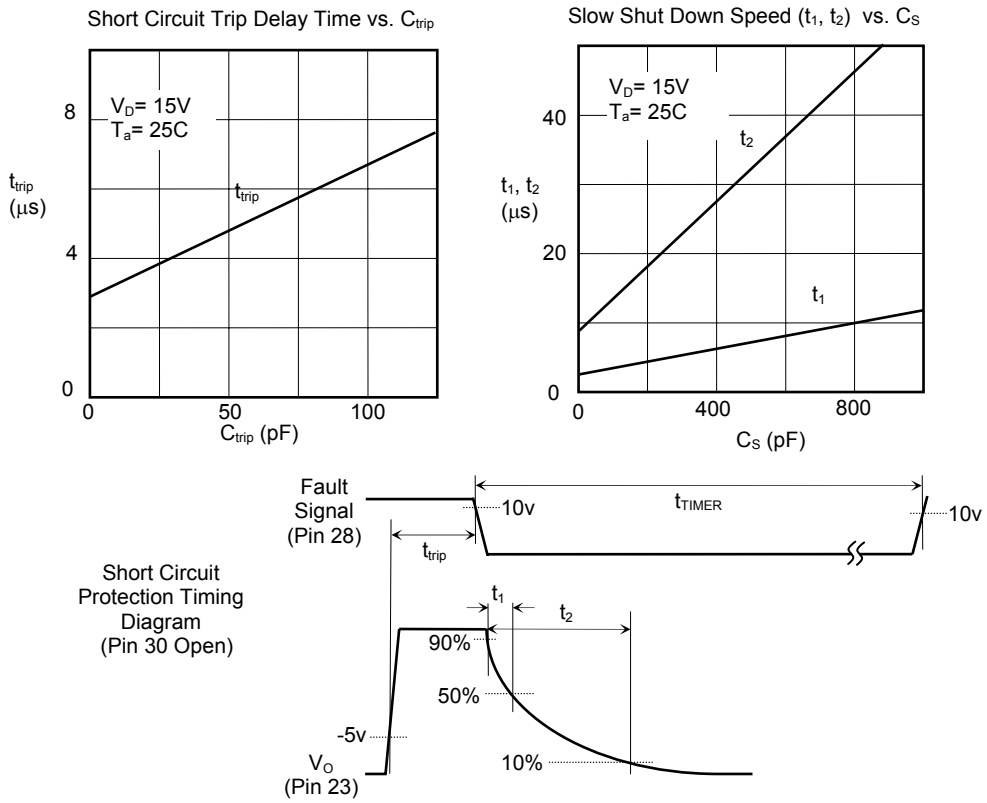


Figure 5: VLA500-01 Adjustment of t_{TRIP} and slow shut down speed

delay time of the IGBT will also increase. If the delay becomes long enough so that the voltage on the detect pin 30 is greater than V_{SC} at the end of the t_{TRIP} delay, the driver will erroneously indicate that a short circuit has occurred. To avoid this condition the VLA500-01 has provisions for extending the t_{TRIP} delay by connecting a capacitor (C_{TRIP}) between pin 29 and V_{EE} (pins 21 and 22). The effect of adding C_{TRIP} on trip time is shown in figure 5. If t_{TRIP} is extended care must be exercised not to exceed the short-circuit withstanding capability of the IGBT module. Normally this will be satisfied for Powerex NF and A-Series IGBT modules as long as the total shut-down time does not exceed 10µs.

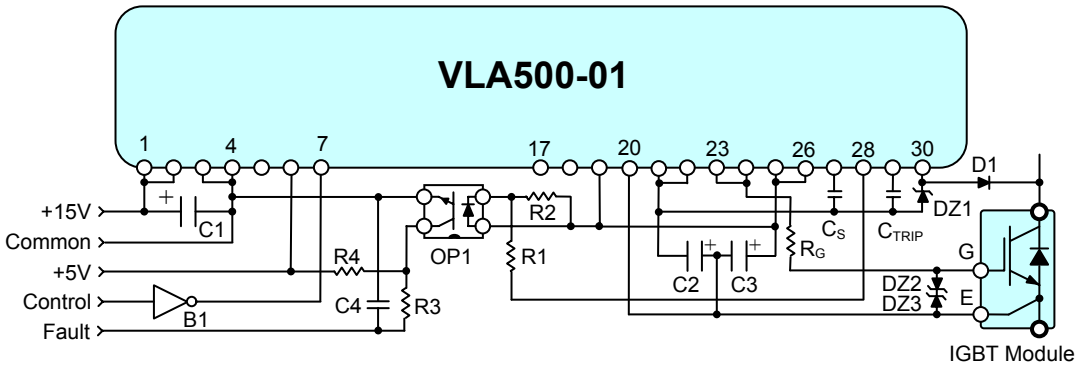
2.4 Adjustment of soft shut-down speed

As noted above the VLA500-01 provides a soft turn off when a short circuit is detected in order to help limit the transient voltage surge that occurs when large short-circuit currents are interrupted. The default shut-down speed will work for most applications so adjustment is usually not necessary. In this case C_S can be omitted. In some applications using large modules or parallel connected devices it may be helpful to make the shut down even softer to minimize transient voltages. This can be accomplished by connecting a capacitor (C_s) between pin 27 and V_{EE} (Pin 21 and 22). The speed of the shut down as a function of C_S is shown in figure 5.

2.5 Disabling short circuit protection

In some applications it may be necessary or desirable to disable the short-circuit protection function of the VLA500-01. This can be accomplished by connecting a 4.7k ohm resistor from pin 30 to pin 20. This will force a low voltage on the detect input (Pin 30) to prevent the driver from detecting desaturation. This is useful if the short-circuit protection is not needed in an application. In this case, the diode D1 and zener DZ1 shown in figure 6 can also be omitted. Disabling the short circuit protection may also be desirable during initial circuit evaluation. With the short circuit protection disabled the drivers output will respond as expected to the input signal even when the IGBT is not connected.

Figure 6: VLA500-01 Typical Application Circuit



Component Selection:

Dsgn.	Typ. Value	Description
D1	0.5 A	V_{CE} detection diode – fast recovery, V_{rrm}>V_{CES} of IGBT being used (Note 1)
DZ1	30V, 0.5W	Detect input pin surge voltage protection (Note 2)
DZ2, DZ3	18V, 1.0W	Gate surge voltage protection
C1	150 μF, 35V	V_D supply decoupling – Electrolytic, long life, low Impedance, 105°C (Note 3)
C2, C3	100-1000 μF, 35V	DC/DC output filter - Electrolytic, long life, low Impedance, 105°C (Note 3,4)
C4	0.01 μF	fault feedback signal noise filter
C_S	0-1000 pF	Adjust soft shut down – Multilayer ceramic or film (see application note)
C_{TRIP}	0-200 pF	Adjust trip time - Multilayer ceramic or film (see application note)
R1	4.7kΩ, 0.25W	fault sink current limiting resistor
R2	3.3kΩ, 0.25W	fault signal noise suppression resistor
R3	1KΩ, 0.25W	fault feedback signal noise filter
R4	4.7K, 0.25W	fault feedback signal pull-up
OP1	NEC PS2501	opto-coupler for fault feedback signal isolation
B1	CMOS Buffer	74HC04 or similar – Must actively pull high to maintain noise immunity

Notes:
(1) The V_{CE} detection diode should have a blocking voltage rating equal to or greater than the V_{CES} of the IGBT being driven. Recovery time should be less than 200ns to prevent application of high voltage to pin 30.
(2) DZ1 is necessary to protect pin 30 of the driver from voltage surges during the recovery of D1.
(3) Power supply input and output decoupling capacitors should be connected as close as possible to the pins of the gate driver.
(4) DC to DC converter output decoupling capacitors must be sized to have appropriate ESR and ripple current capability for the IGBT being driven.

3. Application Circuit for VLA500-01

An example application circuit for the VLA500-01 hybrid gate driver is shown in Figure 6. The complete isolated gate drive circuit can be constructed with as few as eleven external components. This section will describe the main design considerations and component selection for this circuit.

3.1 Control Power Supply

The VLA500-01 requires a single 15V control power supply (V_D) to power its internal circuits. The 15V power supply is connected to the primary side of the hybrid gate driver's built in DC to DC converter at pins 1,2 and 3,4. The control power supply must be decoupled with a capacitor (C1) connected as close as possible to the driver's pins. This decoupling capacitor is necessary to provide a stable, well filtered voltage for the driver's built-in DC to DC converter. When selecting the input decoupling capacitor it is important to ensure that it has a sufficiently high ripple current rating. The example circuit shown in Figure 4 uses a 150μF low impedance type electrolytic for the input decoupling capacitor. This should be sufficient for most applications. It may be possible to use a smaller capacitor if the driver is lightly loaded and/or the main 15V supply filter capacitor is located in close proximity to the driver. The current draw from the 15V supply will vary from about 75mA to almost 500mA

depending on the size of IGBT being driven and the switching frequency. The VLA500-01 data sheet provides typical curves that can be used to calculate the required supply current. The basic procedure is as follows:

(1) Determine the average gate drive current (i_{drive}). The average current required to drive the IGBT is a function of operating frequency, on and off bias voltages, and total gate charge. The average current that must be supplied by the gate driver is given by:

$i_{drive} = Q_G \times f$ Where:
Q_G= is total gate charge
f = is frequency of operation.

The total gate charge (Q_G) can be obtained from the IGBT module data sheet curves. Figure 7 shows a typical gate charge curve. The total gate charge for the transition of gate voltage from zero to +15.3V can be read directly from the curve (7200nC). For the transition from 0 to -8V we can use the initial slope of the Q_G curve as shown in figure 7 to obtain an additional 1200nC. For operation of this device at 20kHz the required supply current is:

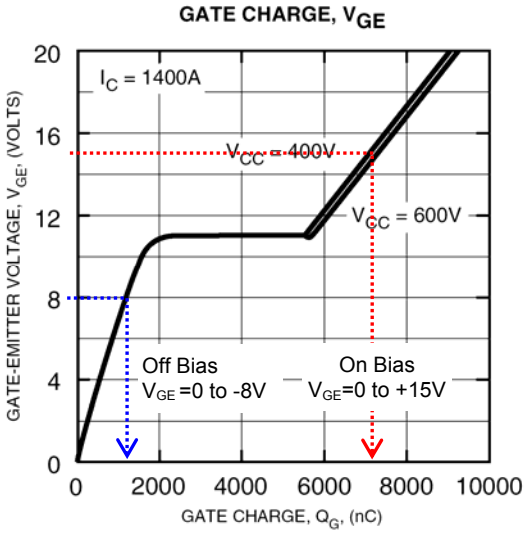


Figure 7: Estimating IGBT Q_G

i_{drive} = (7200nC+1200nC) x 20kHz = 168mA

(2) Calculate the total gate drive power. The power that must be supplied by the VLA500-01 built in DC to DC converter is given by: i_{drive} x (V_{CC} + |V_{EE}|). Where V_{CC} and V_{EE} are the DC to DC converter output voltages specified on the driver data sheet. For a typical application V_{CC} = 16.5V and V_{EE} = -9V so the gate drive power for this example is:

P_G = 168mA x (16.5V + |-9V|) = 4.28W

(3) Calculate the total input power required from the 15V power supply. The VLA500-01 data sheet provides a curve showing the gate driver's efficiency (E_{ta}) versus i_{drive}. This curve is used to account for the losses in the driver's DC to DC converter and output driving stage. At i_{drive} = 168mA the curve indicates an efficiency of approximately 70%. The required total input power (P_T) is calculated using this efficiency as follows:

$P_T = P_G/E_{ta}$ = 4.28W/0.7 = 6.11W

(4) Calculate the required 15V supply current (I_D). The required supply current is simply the total input power divided by the supply voltage.

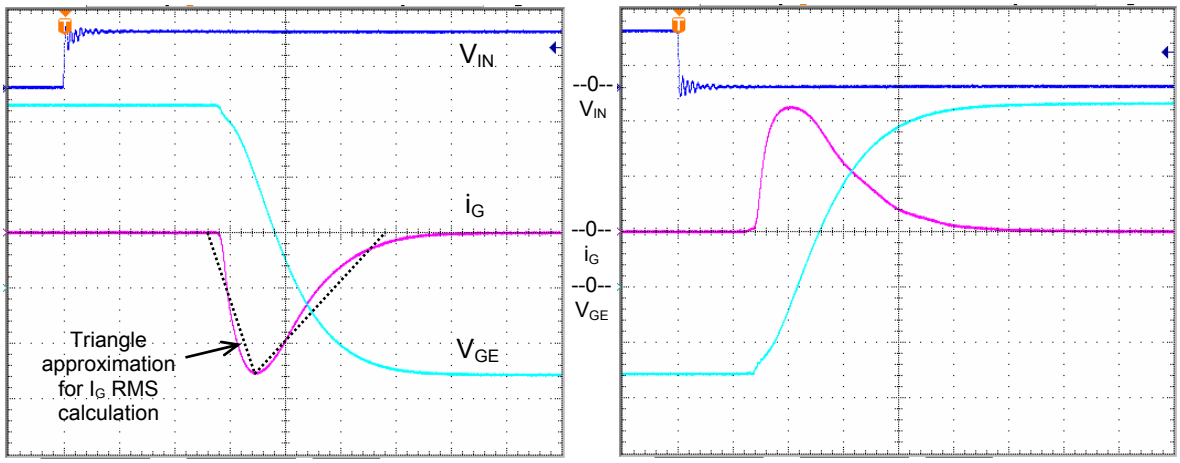
$i_D = P_T/V_D$ = 6.11W/15V = 407mA

3.2 Isolated Power Supplies (V_{CC} and V_{EE})

The VLA500-01 has a built in DC to DC converter that provides isolated gate drive power consisting of +16.4V (V_{CC}) at pin 19 and -9V (V_{EE}) at pins 21 and 22. These supplies share a common ground at pin 20. Transformer coupling provides 2500VRMS isolation between the 15V control supply (V_D) and the gate drive power. This feature allows the VLA500-01 to provide completely floating gate drive that is suitable for high or low side switching.

The gate drive power supplies are decoupled using the low impedance electrolytic capacitors C2 and C3. It is very important that these capacitors have low enough impedance and sufficient ripple current capability to provide the required high current gate drive pulses. The VLA500-01 is designed for use with series gate resistors as small as 1.0ohm. A standard (not low impedance) 100uF electrolytic may have an internal

Figure 8: VLA500-01 Typical Waveform



V_{IN}:5V/div, V_{GE}: 5V/div, i_G:5A/div, t:400ns/div, R_G=1.0ohm, C_L=0.33µF

resistance of one ohm or more. Clearly, this would limit the peak gate driving current to a lower than expected level. Therefore, low impedance capacitors are necessary to deliver high peak gate current.

In addition, electrolytic capacitors also have maximum allowable ripple current specifications due to internal heating effects. If the capacitor's ripple current specification is exceeded, the life of the capacitor can be significantly reduced. In order to estimate the ripple current requirements for the capacitors it is necessary to measure or calculate RMS gate drive current. When measuring RMS gate current be certain that the instrument has a sufficiently high sampling rate to accurately resolve the relatively narrow gate current pulses. Most "true RMS" DMMs are not capable of making this measurement accurately. The RMS gate current can also be estimated from the gate drive waveform. Figure 8 shows a typical gate current waveform. If we assume the turn-on and turn-off pulses are approximately triangular we can estimate RMS gate current using the equations given in Figure 9. Referring to Figure 6 it can be seen that positive gate pulses are supplied by C3 while negative gate pulses are supplied by C2. In most applications the peak gate current is much larger than the average current supplied by the DC to DC converter so it is reasonable to assume that the RMS ripple current in the decoupling capacitor is roughly equal to the RMS gate current. The ripple current in the decoupling capacitors (C2, C3) can be estimated using equations 2 and 3 from Figure 9. For example, if we use a triangular approximation to estimate the RMS current of the turn-

Figure 9: RMS Current Calculations

Eqn. 1: RMS current for repetitive triangular pulses

$$i_{RMS} = i_p \sqrt{\frac{t_p \cdot f}{3}}$$

Where:
i_p = Peak Current
t_p = base width of pulse
f = frequency

Eqn. 2: RMS current for turn-on gate pulses:

$$i_{G(on)}(RMS) = i_p(on) \sqrt{\frac{t_p(on) \cdot f}{3}}$$

Where:
i_p(on) = Peak Turn-On Current
t_p(on) = Base width of On pulse
f = frequency

Eqn. 3: RMS current for turn-off gate pulses:

$$i_{G(off)}(RMS) = i_p(off) \sqrt{\frac{t_p(off) \cdot f}{3}}$$

Where:
i_p(off) = Peak Turn-Off Current
t_p(off)= Base width of Off pulse
f = frequency

Eqn. 4 Total RMS gate current:

$$i_G(RMS) = \sqrt{i_{G(on)}(RMS)^2 + i_{G(off)}(RMS)^2}$$

Or assuming $i_{G(off)} = i_{G(on)}$
(On and Off current pulses are symmetric) the RMS gate current is:

$$i_G(RMS) = i_p \sqrt{\frac{2 \cdot t_p \cdot f}{3}}$$

Where:
i_p = Peak Gate Current
t_p = base width of gate drive pulse
f = frequency

off pulses shown in Figure 8 we see that $i_p(off)$=12A and $t_p(off)$=1440ns. If the switching frequency f=20Khz then using equation 3 of Figure 9 the RMS ripple current in C2 is approximately:

$$i_{G(off)}(RMS) = i_p(off)\sqrt{\frac{t_p(off)\cdot f}{3}} = 12A\sqrt{\frac{1280ns\cdot 20kHz}{3}} = \mathbf{1.11\ ARMS}$$

Generally it is a good idea to select a capacitor with a maximum ripple current rating larger than the calculated current. For this example a low impedance 1000uF electrolytic capacitor such as Panasonic type EEU-FC1V102 with a ripple current rating of 1.95A would be an appropriate choice. If the application is operating at lower frequency or lower peak current (larger R_G) it is possible to reduce the size of the decoupling capacitors C2 and C3. However, keep in mind that larger capacitors with higher ripple current ratings will provide longer life and are therefore always desirable. The only penalties for using larger than necessary capacitors are the size and cost.

3.3 Gate Drive and Resistance (R_G)

The V_{EE} and V_{CC} supplies are connected to the drivers output stage to produce gate drive at pins 23 and 24. The gate drive current is adjusted by selecting the appropriate series gate resistance (R_G). R_G will normally be adjusted to provide suitable drive for the IGBT module being used. A smaller R_G will provide faster switching and lower losses while a larger R_G will provide reduced transient voltages and switching noise. Typically, larger modules will require a smaller R_G and smaller modules will use a larger R_G. For most Powerex IGBT modules the minimum recommended R_G can be found in the conditions for the switching time specifications on the module's data sheet. In most applications the optimum R_G will be somewhere between the data sheet value and ten times that value. Keep in mind that the minimum allowable R_G for the VLA500-01 is 1.0 ohm. An R_G of less than 1.0 ohm may cause the peak output current to exceed the driver's 12A limit.

When driving large IGBT modules at high frequency the power dissipated in the series gate resistor R_G can be substantial. The power dissipation can be estimated using equation 4 from Figure 9. For the example waveform shown in Figure 8 the approximate RMS gate current is:

$$i_G(RMS) = i_p\sqrt{\frac{2\cdot t_p\cdot f}{3}} = 12A\sqrt{\frac{2\cdot 1280ns\cdot 20kHz}{3}} = \mathbf{1.57\ ARMS}$$

The series gate resistor in this example was 1.0 ohm so the total power dissipation is:

$P = i^2 \cdot R = 1.57ARMS^2 \cdot 1ohm =$ **2.46W**

So in this case, at least a 3W resistor is required. The gate drive circuit layout must be designed so that the additional heat produced by the gate resistor does not overheat nearby components.

Protection against gate voltage surges is provided by back to back zener diodes DZ2 and DZ3. These zener diodes also help to control short circuit currents by shunting miller current away from the gate. These zeners must be capable of supporting high pulse currents. Therefore, devices with a minimum 1W rating are recommended.

Additional information on gate drive requirements for IGBT modules and selection of R_G can be found in Powerex IGBT module application notes.

3.4 Collector Voltage Sensing

Short circuit protection is provided by means of desaturation detection as described in section 2 above. The collector voltage of the IGBT is detected through the high voltage blocking diode (D1). The blocking voltage of D1 should be equal to or greater than the V_{CES} rating of the IGBT being used. For applications using high voltage IGBTs it may be necessary to use series connected diodes to achieve the desired blocking voltage. D1 must be ultra fast recovery to minimize the surge applied to the gate driver's detect input (Pin 30). The zener

diode DZ1 provides additional protection of the gate driver's detect input from voltage surges during reverse recovery of the high voltage blocking diode.

3.5 Input Circuit

The input circuit between pins 6 and 7 consists of the built-in high speed opto coupler's LED in series with a 180Ω resistor. This combination is designed to provide approximately 16mA of drive current for the optocoupler when a 5V control signal is applied. In most applications pin 6 will be tied directly to the 5V logic power supply. An ON signal (gate output high) is generated by pulling pin 7 to ground using a CMOS buffer capable of sinking at least 16mA (74HC04 or similar). In the off state the buffer should actively pull pin 7 high to maintain good noise immunity. Open collector drive that allows pin 7 to float will degrade common mode noise immunity and is therefore not recommended.

If a different control voltage is desired an external current limiting resistor can be added. The value of the external resistor can be calculated by assuming the forward voltage drop of the optocoupler's photodiode is approximately 1.5V and that the on state voltage drop across the driver is about 0.6V. For example, if 15V drive is desired, the required external resistor would be: (15V-1.5V-0.6V) ÷ 16mA - 180Ω = 630Ω. To maintain good common mode noise immunity this resistor should always be connected in series with pin 7. Connecting the resistor in series with pin 6 will degrade the common mode noise immunity of the gate driver.

3.6 Fault Signal

If the gate driver's short-circuit protection is activated it will immediately shut down the gate drive and pull pin 28 low to indicate a fault. Current flows from Vcc (pin 19) through the LED in fault isolation opto (OP1) to pin 28. The transistor in the fault isolation opto turns on and pulls the fault signal line low. During normal operation the collector of the opto transistor (OP1) is pulled high to the +5V logic supply by the resistor R3. When a fault is detected the hybrid gate driver disables the output and produces a fault signal for a minimum of 1ms. Any signal on the fault line that is significantly shorter than 1ms can not be a legitimate fault so it should be ignored. Therefore, for a robust noise immune design, it is recommended that an RC filter with a time constant of approximately 10us be added (R3, C4). This opto isolated fault signal can now be used by the controller to detect the fault condition. If the short circuit protection function is not being used and has been properly disabled as described in section 2.5 then OP1, R1 and R2 can be omitted and pin 28 left open.

4.0 Additional Information

Additional detailed information on using the VLA500-01 gate driver can be found on the device data sheet. The BG2A gate drive reference design shown in figure 10 is available for prototype evaluation. The BG2A is a complete two channel gate drive reference design printed circuit board that uses the VLA500-01. Full documentation for the BG2A is available from the Powerex website. For additional general information on IGBT module gate drive requirements please refer to Powerex IGBT module application notes.

Figure 10: BG2A Reference Design